Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 7, 18, and 24 have been amended. No claims have been canceled or added. Claims 3, 4, 9, 20, and 27 were previously canceled. Claims 10-17 were previously withdrawn. Therefore, claims 1, 2, 5-8, 18, 19, 21-26, 28, and 29 are presented for examination.

Specification

The specification is objected to for the following reasons:

First, the title is objected to as not being descriptive. The title is currently amended per the Examiner's suggestion to incorporate into the title the attaching of a breakpoint bit to each instruction. As this is the third time the title is being amended, applicant feels they have addressed the Examiner's concerns and **that the title is presently fully descriptive per the guidelines set out by the patent rules and regulations**. If the Examiner still does not find the title to be descriptive, applicant invites the Examiner to contact the applicant to discuss further any changes the Examiner feels should be made to the title. Otherwise, applicant respectfully requests the withdrawal of the present objection to the title.

Second, the abstract of the disclosure is objected to as the Examiner states it does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). However, applicant submits that the application as filed on March 31, 2004, included an Abstract that did in fact commence on a separate sheet. Therefore, applicant respectfully disagrees with the present objection to the Abstract and requests its withdrawal.

Lastly, the claims are objected to due to the feature of the three debug register bit fields, for example in claim 1. The Examiner states that these fields are part of the processor control status register and are not added or attached to the control status register. However, the claims presently recite that the debug register fields are **manipulated** (see, e.g., claims 1, 18, and 24) and not added or attached as the Examiner asserts. As such, the present objection to the claims is moot and applicant respectfully requests its withdrawal.

Drawings

The drawings have been amended to place them in better form for allowance. Specifically, Figure 6 is amended to label the entire component of Figure 6 as the "ISP Control Status Register" per the Examiner's suggestion in the Office Action. Figure 8A has been amended to add an arrow from step 855 to step 860 per the Examiner's suggestion. Figure 8B is amended to change the language "LDTI Into Debug Instruction Register" to "LDTI From Debug Instruction Register" on the left side of the figure. In addition, Figures 8C and 8D have been amended to have a more formal appearance. As a result of the above amendments, applicant respectfully requests that the present objection to the drawings be withdrawn.

Claim Objections

Claims 1, 7, 18, and 24 were objected to for minor informalities. Applicant has amended claims 1, 7, 18, and 24 to correct the minor informalities. As such, applicant respectfully requests the withdrawal of the present claim objections.

35 U.S.C. §112 Rejection

Claims 1-2, 5-8, 18-19, 21-26, and 28-29 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claims 1, 18, and 24 recite the limitation "the particular instruction." There is insufficient antecedent basis for this limitation. Also, claim 24 recites the limitation "the apparatus." There is also insufficient antecedent basis for this limitation. Claims 1, 18, and 24 have been amended to address and correct the antecedent basis problems of the present §112 rejection. As such, applicant respectfully requests that the present §112 rejection be withdrawn.

35 U.S.C. §103 Rejection

Glew, IBM and Deng

Claims 1-2, 5-8, 18-19, 21-26 and 28-29 are rejected under 35 U.S.C. 103(e) as being unpatentable over Glew, et al., U.S. Patent No. 5,694,589 ("Glew"), in view of IBM Technical Disclosure Bulletin NN8907370 (as previously cited and herein referred to as IBM), and in further view of Deng et al., U.S. Patent No. 6,951,416 ("Deng"). Applicant submits that the present claims are patentable over Glew and IBM in view of Deng.

Glew discloses code breakpoint detection logic for a superscalar microprocessor. (Glew at Abstract.) IBM discloses a technique that provides a breakpoint function in a processor without the use of extra comparison logic and with minimal delay. (IBM at Disclosure Text.) Deng discloses debugger circuitry that is implemented on the microcontroller itself and that may break application program execution upon detection of a

specified condition, display internal register values to the user, and continue the application program execution. (Deng at col. 2, ll. 37-41.)

Claim 1, as amended, recites:

> An apparatus comprising:
> a memory;
> a plurality of processors coupled to the memory; and
> a controller coupled to the memory and the plurality of processors, the controller to execute a debug process that:
> attaches at least one breakpoint bit field comprising a single bit directly to one or more instructions of the plurality of processors, the breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of an instruction of the one or more instructions that the breakpoint bit field is attached without having to perform an address comparison;
> manipulates at least three debug register bit fields of at least one processor control status register, the at least three register bit fields comprising a run field, a single step field, and a debug enable field that each comprise a single bit; and
> accesses an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM (LDTI) instruction and a Load from Instruction RAM (LDFI) instruction.

Applicant submits that Glew does not disclose or suggest a debug process that manipulates at least three debug register bit fields of at least one processor control status register, the at least three register bit fields comprising ***a run field, a single step field, and a debug enable field that each comprise a single bit***, as recited in claim 1 (emphasis added). The Examiner acknowledges this when stating that "Glew has further not taught that the debug process manipulates at least three debug register bit fields...comprising a run field, a single step field and a debug enable field." (Office Action at pg. 7, pt. 18(d).) However, the Examiner does rely on Deng to teach such a feature.

Applicant further submits that Deng also does not disclose or suggest a debug process that manipulates at least three debug register bit fields of at least one processor control status

register, the at least three register bit fields comprising ***a run field, a single step field, and a debug enable field that each comprise a single bit***, as recited in claim 1 (emphasis added). The Examiner cites Deng at Figure 16 to teach this feature and specifically states with respect to Figure 16 of Deng that "note field 208, which is a debug enable field, field 206, which is a single-step field, and field 202 (BE1, BE2, BE3, or BE4), which is a run field." (Id.) Yet, applicant submits that Deng actually does not disclose or suggest a run field comprising a single bit.

The Examiner equates the run field of claim 1 with field 202 (BE1, BE2, BE3, or BE4) of Figure 16 of Deng. However, field 202 is actually a plurality of breakpoint enable fields spanning 4 bits, not a run field spanning a single bit. The run field of claim 1 is not the same as the breakpoint field in claim 1. The disclosure of Deng in Figure 16 provides for multiple breakpoint enable bits for particular instructions, rather than for a run field of a single bit that would cover execution of instructions in an entire processor. As such, Deng does not disclose or suggest the cited feature of claim 1.

Finally, applicant submits that IBM does not disclose or suggest the cited feature of claim 1. The Examiner does not rely on IBM to teach this feature, nor can applicant find any disclosure or suggestion of the feature anywhere in IBM. As such, IBM does not disclose or suggest the cited feature of claim 1.

In conclusion, none of Glew, IBM, or Deng, individually or in combination, discloses or suggests the above-cited feature of claim 1. As a result, claim 1, as well as its dependent claims is patentable over Glew and IBM in view of Deng.

Independent claims 18 and 24 also recite the above-cited feature of claim 1. As a result, claims 18 and 24, as well as their respective dependent claims, are also patentable over Glew and IBM in view of Deng.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: May 30, 2008

Ashley R. Essick
Reg. No. 55,515

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(303) 740-1980